



APPLICATION NO.

MP0020

09/737,743

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT

Sehat SUTARDJA

DATE SUBMITTED TO USPTO: October 7, 2005

FILING DATE

GROUP

12/18/2000

2631

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

• EXAMINER
INITIALS

Dunning, Jim, "An All-Digital Phase-Locked Loop with 50-Cycle Lock Time Suitable for High-Performance Microprocessors," IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 30, No. 4, April 1995, pp. 412-422

Maneatis, John G., "FA 8.1: Low-Jitter and Process-Independent DLL and PLL Based on Self-Biased Techniques"

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Goldberg, Lee, "Gigabit Ethernet PHY Chip Sets LAN Speed Record for CopperStory," TECH INSIGHTS, November 16, 1998, 6 pages

EXAMINER

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DATE CONSIDERED

6/9/06

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U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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